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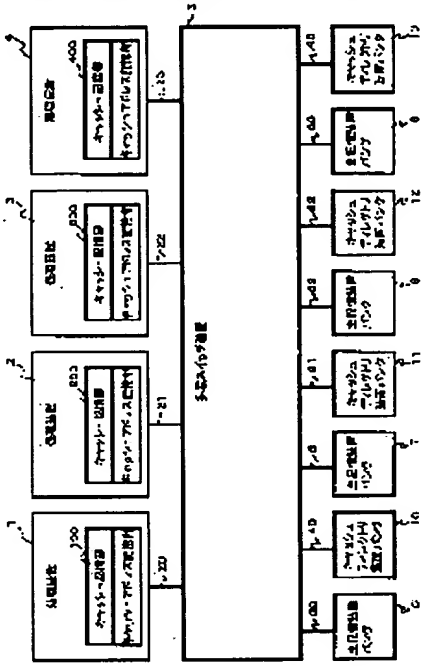
## (54) INFORMATION PROCESSOR FOR EXECUTION OF CACHE COINCIDENCE ASSURANCE CONTROL

(57)Abstract:
PROBLEM TO BE SOLVED: To provide an information processor which can suppress the physical quantity of hardware that is related to the cache coincidence assurance control and also can reduce the effect to the system performance.
SOLUTION: This information processor consists of plural processors (IP) 1, 2, 3 and 4, a multistage switching device(SW) 5, the banks 6, 7, 8 and 9 of a main storage(MS) which have different address spaces and apply the configurations to operate in parallel to each other and the banks 10, 11, 12 and 13 of a cache directory device (CD) which have plural column groups respectively and apply the bank configurations to operate independently of each other. The CD is divided into banks according to the column of a cache address storage part of each IP.



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